# A NONLINEAR MODEL OF THE POWER MESFET INCLUDING TEMPERATURE AND BREAKDOWN EFFECTS

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## ABSTRACT

The paper discusses a new large-signal MESFET model based on d.c., S-parameter and nonlinear measurements. Physical constraints incorporated in the constitutive relations guarantee the model consistency in large-signal operation and improve the reliability of the parameter extraction process. Forward and reverse (breakdown) gate conduction effects are modeled from nonlinear data. Extensive comparisons with experimental results are presented.

## INTRODUCTION

In the simulation of nonlinear microwave circuits, the determination of suitable models for the active devices represents one of the most critical issues. From the general-purpose CAD viewpoint, functional models extracted from measured information often represent the most appropriate choice. Such models are efficiently handled by nonlinear simulators, do not require the storage of large measured databases, and are fully identified by a relatively small number of scalar parameters. The latter is a very important advantage in view of the realization of extensive nonlinear device libraries, such as required for commercial software and foundry services. From the engineering viewpoint, the usefulness of a model is obviously established by its ability to accurately reproduce the device performance under the broadest possible range of operating conditions, from d.c. to microwave, from small to large signal. The achievement of this result depends on the type and amount of data used to identify the model, on the quality of the parameter extraction process, and on the physical likelihood of the model, that is, its ability to provide in a synthetic way a physically consistent global description of the complex phenomena that determine the device performance.

In this paper we propose a new modeling procedure for power MESFETs, based on the introduction of physical constraints in order to improve the physical likelihood of the model. Four kinds of constraints are imposed, namely, symmetry, continuity, conservation, and dispersion constraints. Rather than being a priori postulated, an equivalent circuit topology is built up stepwise, starting from a kernel describing the quasi-static charge storage process, by adding subsequent shells that globally account for various aspects of the measured behavior. The model constitutive relations are expressed by closed-form parametrized equations depending on three state variables (two voltages and one temperature), and are devised in such a way as to formally incorporate the physical constraints. This reduces the a priori uncertainty on the model parameters, and thus results in a more reliable and repeatable parameter identification. The measured database includes d.c., S-parameter, and large-signal information. The role of S-parameter fitting - usually the weak link of conventional modeling approaches - is limited to finding starting points for the true extraction process, or to obtaining minor refinements of already known parameters within narrow ranges of variation. Nonlinear data is used to identify suitable models for the forward and reverse (breakdown) gate conduction currents. This allows the two principal physical mechanisms responsible for saturation [1] to be incorporated in the device description. The result is a universal model that can accurately reproduce the measured d.c., small-signal, and nonlinear device performance over a broad range of voltages and temperatures, including negative and zero drain-source voltages.

## MODEL TOPOLOGY AND CONSTITUTIVE RELATIONS

The model topology is shown in fig. 1. The model is formulated parametrically in terms of one thermal state variable (SV) T(t) representing the peak device temperature, and three electrical SV $x_1(t)$, $x_2(t)$, $x_3(t)$, having the physical dimensions of voltages, and satisfying the constraint $x_3(t) = x_1(t) - x_2(t)$. Thus only two electrical SV are independent, so that the constitutive relations can be formulated in terms of a state vector

$$\mathbf{x}(t) = [x_1(t), x_2(t), T(t)]^{tr} \tag{1}$$

where $^{tr}$ denotes transposition. $x_1(t)$, $x_2(t)$, $x_3(t)$ should be interpreted as fictitious voltages, i.e., do not coincide with voltages actually measurable between specific couples of points inside the device. The model topology satisfies the symmetry constraint originating from the observation that in the FET active region the source and drain terminals are normally indistinguishable, and any asymmetries are due to the electrode shapes and positions. Also, this symmetrical structure lends itself naturally to the development of a two-sided FET model, equally valid for positive, zero, and negative values of the drain-source voltage [2]. Continuity constraints are an obvious corollary of this requirement, since the model constitutive relations must be continuous together with their derivatives at zero drain-source voltage, in order to ensure the consistency of the device descriptions in the three regions.

The logical construction of the model starts from a kernel (shell 1) representing the quasi-static charge storage process. The latter is described as a standard electrostatic phenomenon, and is thus charge- and energy-conservative. As a consequence, it is completely characterized by a state-dependent energy function $E[\mathbf{x}]$ [2], [4]. A suitable expression of the energy function was reported in [3]. The terminal charges are then expressed by the equations

$$q_G[\mathbf{x}] = \frac{\partial E[\mathbf{x}]}{\partial x_1}\ ; \qquad q_D[\mathbf{x}] = \frac{\partial E[\mathbf{x}]}{\partial x_2} \qquad q_S[\mathbf{x}] = -q_G[\mathbf{x}] - q_D[\mathbf{x}] \tag{2}$$

so that the quasi-static displacement currents are given by

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$$i_{QZ}(t) = \frac{\partial q_Z[\mathbf{x}(t)]}{\partial t} \tag{3}$$

where the subscript "Z" stands for G, D or S.

Any deviations of the actual charge-storage process from the ideal electrostatic model will be referred to as nonquasi-static charge-storage effects. These effects are globally modeled by introducing the nonlinear charging resistances $R_{CG}[\mathbf{x}]$, $R_{CD}[\mathbf{x}]$, $R_{CS}[\mathbf{x}]$ connected in series to the terminals of shell 1 (see fig. 1). In order to justify this choice, we introduce the differential capacitance matrix $\mathbf{C}[\mathbf{x}]$ and the resistance matrix $\mathbf{R}[\mathbf{x}]$ defined by

$$\mathbf{C}[\mathbf{x}] = \begin{bmatrix} \dfrac{\partial^2 E[\mathbf{x}]}{\partial x_1^2} & \dfrac{\partial^2 E[\mathbf{x}]}{\partial x_1 \partial x_2} \\ \dfrac{\partial^2 E[\mathbf{x}]}{\partial x_1 \partial x_2} & \dfrac{\partial^2 E[\mathbf{x}]}{\partial x_2^2} \end{bmatrix} \tag{4}$$

$$\mathbf{R}[\mathbf{x}] = \begin{bmatrix} R_{CG}[\mathbf{x}] + R_{CS}[\mathbf{x}] & R_{CS}[\mathbf{x}] \\ R_{CS}[\mathbf{x}] & R_{CD}[\mathbf{x}] + R_{CS}[\mathbf{x}] \end{bmatrix}$$

Considering then a small-signal sinusoidal regime of (angular) frequency ω superimposed on a quiescent point $\mathbf{x_0}$, and assuming that $\omega^2\mathbf{C}(\mathbf{x_0})\mathbf{R}(\mathbf{x_0})\mathbf{C}(\mathbf{x_0})\mathbf{R}(\mathbf{x_0})$ can be neglected and that temperature changes are relatively slow, the common-source admittance matrix at the terminals of shell 2 is approximately given by

$$\mathbf{Y_Q}(\omega;\mathbf{x_0}) \approx j\omega\mathbf{C}(\mathbf{x_0}) + \omega^2\mathbf{C}(\mathbf{x_0})\mathbf{R}(\mathbf{x_0})\mathbf{C}(\mathbf{x_0}) \tag{5}$$

This is the same effect produced by the nonlinear relaxation time model [5], [6]. For $x_2 \geq 0$ the following constitutive relations are adopted for the charging resistors:

$$\begin{aligned} R_{CG}[\mathbf{x}] &= R_{G0}(1 + K_{G1}x_1)^{E_{G1}}\,(1 + K_{G2}x_2)^{E_{G2}} \\ R_{CD}[\mathbf{x}] &= R_{D0}\,(1 + K_{D2}x_2)^{E_{D2}} \\ R_{CS}[\mathbf{x}] &= R_{S0} \end{aligned} \tag{6}$$

where $R_{G0}$, $R_{D0}$, $R_{S0}$, $K_{G1}$, $K_{G2}$, $K_{D2}$, $E_{G1}$, $E_{G2}$, $E_{D2}$ are model parameters. Similar results may be obtained for the common-drain configuration by interchanging the source and drain terminals in the way discussed in [2].

In order to complete the intrinsic FET model, a set of conduction currents must be added to the realistic (nonquasi-static) displacement currents modeled as discussed above. These currents are globally described by a number of nonlinear current sources (shell 3 in fig. 1) connected in parallel to the terminals of shell 2. The contributions taken into account are the channel current ($i_{DS}[\mathbf{x}]$), the forward currents of the gate-source and gate-drain diodes ($i_{GS}[\mathbf{x}]$, $i_{GD}[\mathbf{x}]$), and the drain-gate (source-gate in the reverse mode of operation) breakdown currents ($i_{DGB}[\mathbf{x}]$, $i_{SGB}[\mathbf{x}]$). The channel source $i_{DS}[\mathbf{x}]$ must account for the well-known low-frequency dispersion phenomena due to trapping effects [7]. This problem is solved by introducing two independent determinations of $i_{DS}[\mathbf{x}]$, namely, a d.c. channel source $i_{DC}[\mathbf{x}]$, and a microwave channel source $i_{RF}[\mathbf{x}]$. The adopted constitutive relations were reported in [4].

The constitutive relations for $i_{DC}$ and $i_{RF}$ must be suitably combined to compute the channel current. This can be done, for instance, by means of dynamic operators [7]. However, in most practical cases the cutoff frequency of the low-frequency dispersion phenomena is of the order of a few hundred kHz. If all the spectral components of the signal waveforms have frequencies larger than this (which is virtually always the case for microwave applications), the following simple expression may be adopted

$$\begin{aligned} i_{DS}(t) &= i_{RF}[x_1(t-\tau), x_2(t-\tau), T(t)] + \\ &+ \exp\left(-\kappa\frac{X_{rms}}{X_{2b}}\right)\left\{i_{DC}[X_{1b}, X_{2b}, T(t)] - i_{RF}[X_{1b}, X_{2b}, T(t)]\right\} \end{aligned} \tag{7}$$

where $X_{1b}$, $X_{2b}$ define the FET bias point, $X_{rms}$ is the r.m.s. value of the RF component of $\|\mathbf{x}(t)\|$, and κ is a model parameter. The exponential function in (7) provides a smooth transition between d.c. and RF operation, and ensures the model consistency under small- and large-signal conditions. τ has the meaning of a transfer delay whose purpose is to globally account for the channel delay and for the distributed effects arising from the finite gate width. Note that with (7) the effects of a state-dependent transfer delay can easily be accounted for by letting $\tau = \tau[\mathbf{x}]$. For $x_2 \geq 0$ the adopted constitutive relation is

$$\tau[\mathbf{x}] = \tau_0 + (\delta_1 x_1 + \delta_2 x_2)[1 + A_\tau(T - T_R)] \tag{8}$$

where $\tau_0$, $\delta_1$, $\delta_2$ are model parameters and $T_R$ is a reference temperature. The extension to $x_2 < 0$ is carried out in the way discussed in [2]. It has long been recognized that in a MESFET the transfer delay is temperature and voltage dependent [8]. Nevertheless, this effect is ignored in most currently available nonlinear models, despite the fact that a state-dependent delay time is the only way of accurately simulating some aspects of power amplifier performance, such as the phase droop in pulsed-RF operation [9]. The forward gate conduction currents have been found to be adequately modeled by the simple Schottky-barrier laws

$$\begin{aligned} i_{GS}[\mathbf{x}] &= I_{G0}\left[\exp\left(\frac{q_e x_1}{nK_B T}\right) - 1\right] \\ i_{GD}[\mathbf{x}] &= I_{G0}\left[\exp\left(\frac{q_e x_3}{nK_B T}\right) - 1\right] \end{aligned} \tag{9}$$

where $q_e$ is the electron charge and $K_B$ is Boltzmann's constant. The diode parameters are assumed to be equal due to the symmetry constraint. Also, the model performance has been found to be only marginally influenced by the dependence of the diode parameters on the SV, so that $I_{G0}$, n are simply treated as (constant) model parameters. A number of experiments have been carried out in order to devise a simple model allowing the effects of drain-gate breakdown to be adequately described. Best results have been obtained by introducing a state-dependent threshold of the form

$$B_{DG}[\mathbf{x}] = c_{DG}x_1 + d_{DG}x_1^2 + e_{DG}x_1^3 + f_{DG}x_2 + g_{DG} \tag{10}$$

and letting $i_{DGB}[\mathbf{x}] = 0$ for $B_{DG}[\mathbf{x}] \leq 0$, and

$$i_{DGB}[\mathbf{x}] = I_{DG0}[1 + A_{DGB}(T - T_R)]\left\{B_{DG}[\mathbf{x}]\right\}^{(a_{DG} - b_{DG}x_1)} \tag{11}$$

for $B_{DG}[\mathbf{x}] > 0$. $I_{DG0}$, $a_{DG}$, $b_{DG}$, $c_{DG}$, $d_{DG}$, $e_{DG}$, $f_{DG}$, $g_{DG}$ are model parameters. A similar expression can be used to model source-gate breakdown.

Finally, the outermost shell (shell 4 in fig. 1) contains the series R-L parasitics of the FET terminals. The inductances

are considered constant (linear), but the resistances are treated as nonlinear components in order to account for the role exchange of the source and drain terminals when the drain-source voltage changes sign [2].

## MODEL PARAMETER EXTRACTION AND RESULTS

The parameter extraction for the model of fig. 1 starts with the identification of the extrinsic parasitics by fitting S-parameters measured in cold-FET and pinched-off conditions. This produces reasonably good values for the inductances, but only coarse approximations for the resistances [10]. In order to remove this uncertainty, we observe that as long as (5) holds, the **Y** matrix of the intrinsic FET (at the terminals of shell 3) at a generic quiescent point $\mathbf{x_0}$ takes on an expression of the form

$$\mathbf{Y}(\omega;\mathbf{x_0}) \approx \mathbf{D}(\mathbf{x_0})\mathbf{G}(\mathbf{x_0}) + j\omega\mathbf{C}(\mathbf{x_0}) + \omega^2\mathbf{N}(\mathbf{x_0}) \qquad (12)$$

where the matrices $\mathbf{G}(\mathbf{x_0})$, $\mathbf{C}(\mathbf{x_0})$, $\mathbf{N}(\mathbf{x_0})$, are real and frequency independent, $\mathbf{C}(\mathbf{x_0})$, $\mathbf{N}(\mathbf{x_0})$, are symmetric, and $\mathbf{D}(\mathbf{x_0})$ is the 2 x 2 diagonal matrix

$$\mathbf{D}(\mathbf{x_0}) = \mathrm{diag}\left[1 \quad \exp\left\{-j\omega\tau(\mathbf{x_0})\right\}\right] \qquad (13)$$

The second step of the extraction process is thus to optimize the extrinsic parasitics in such a way that (12), (13) be satisfied at all quiescent points of interest. It has been found that this goal can be met with excellent accuracy for a wide variety of devices up to frequencies of the order of 26 GHz. This method provides very sharply defined values of the extrinsic parasitics, of the state-dependent coefficients $\mathbf{G}[\mathbf{x}]$, $\mathbf{C}[\mathbf{x}]$, $\mathbf{N}[\mathbf{x}]$, and of the time delay $\tau[\mathbf{x}]$. A few representative results obtained for a 1-mm FET with 10 gate fingers (Alenia P11) are shown in fig. 2. The real and imaginary parts of the intrinsic y-parameters extracted after optimizing the parasitics are almost exactly quadratic and linear functions of ω, respectively, so that $\mathbf{G}[\mathbf{x}]$, $\mathbf{C}[\mathbf{x}]$, $\mathbf{N}[\mathbf{x}]$, are truly frequency independent. The small errors on the real parts observed above 22 GHz are nonquasi-static effects due to higher-order terms in ω that are neglected by the approximation (5). However, these discrepancies may be completely removed by the subsequent optimization of the charging resistances, as discussed below.

The next step is to identify the parameters of the energy function. For this purpose, the capacitance matrix is formally expressed by means of the first of (4). The parameters are then found by fitting such expressions to the extracted $\mathbf{C}[\mathbf{x}]$ over all the available quiescent points. A comparison of (5) and (12) then yields

$$\mathbf{R}[\mathbf{x}] = \mathbf{C}^{-1}[\mathbf{x}]\,\mathbf{N}[\mathbf{x}]\,\mathbf{C}^{-1}[\mathbf{x}] \qquad (14)$$

Since $\mathbf{C}[\mathbf{x}]$, $\mathbf{N}[\mathbf{x}]$ are known, (14) provides reasonable starting points (low-frequency limits) for the charging resistances of shell 2. The latter are then refined by fitting the Y-parameters at the terminals of shell 2 (exactly computed from the circuit topology) to those extracted from measurements.

The final step is the identification of the nonlinear current sources. For $x_2 \geq 0$, the common-source differential transconductance and output conductance are given by

$$g_m[\mathbf{x}] = \frac{\partial i_{RF}[\mathbf{x}]}{\partial x_1} \;; \qquad g_{out}[\mathbf{x}] = \frac{\partial i_{RF}[\mathbf{x}]}{\partial x_2} \qquad (15)$$

The conductances are formally expressed by means of (15), and the model parameters are found by fitting such expressions to the corresponding entries of the extracted conductance matrix $\mathbf{G}[\mathbf{x}]$ over all the available quiescent points. Note that this procedure exactly enforces the current conservation constraint [7]. The extension to $x_2 < 0$ is carried out in the way discussed in [2]. The d.c. current source $i_{DC}[\mathbf{x}]$ is directly identified by fitting d.c. measured data. For all constitutive relations, the temperature coefficients are determined by comparing the results derived from measurements taken at two different ambient temperatures, and simultaneously accounting for the device self-heating in the way discussed in [4].

d.c. data cannot be normally used to extract the parameters of the forward diode currents (9) and of the breakdown current source (11), because biasing the device in the forward or reverse gate conduction regions may result in permanent damage. In practice, the device is virtually always biased at negative (or occasionally zero) gate voltage, and far from breakdown; forward and reverse gate conduction may nevertheless occur under strong RF drive for a short fraction of the period. In fact, these are the two main saturating mechanisms of the MESFET [1]. For the above reasons only the RF determinations of the current sources (9), (11) are of interest, even though these sources are likely to exhibit low-frequency dispersion in a way similar to the channel current source. The conclusion is that large-signal RF measurements should be used to generate the experimental information required for the identification of (9) and (11). A detailed investigation was carried out in order to establish the type of data that is best suited for a reliable identification of the model parameters. The result is that with the functional form (11) and the simple diode laws (9), a good model for general-purpose CAD applications can be obtained by fitting at two bias points the power-added efficiency (PAE) and the d.c. component of the gate current measured as a function of input power. The fitting is carried out by harmonic-balance (HB) based optimization with respect to the unknown model parameters, with the measured data replacing the design goals. The optimization takes simultaneously into account a number of power levels arbitrarily selected within the range of interest, and is based on the exact derivatives of the objective function with respect to the nonlinear device parameters that were developed in [11]. Excellent results have been obtained in this way for several power devices. A few representative examples are reported in figs. 3 - 4. Fig. 3a) shows a typical comparison between the measured and modeled power-added efficiency (PAE) of the Alenia P11 with 50 Ω input and output terminations. The PAE computed by the model in the absence of limiting mechanisms is also shown for reference in this figure. Fig. 3b) shows a comparison between the measured and modeled output power and d.c. gate current of the Alenia P11 under the same conditions. The excellent performance of the model well into the power saturation region is evident from these figures. Fig. 4 shows that the model can also accurately predict the harmonic levels measured under large-signal sinusoidal drive up to the 4-th harmonic.

The small-signal performance of the device is equally well predicted by the model over a broad range of quiescent points. Fig. 5 shows a typical comparison between measured (black squares) and modeled (solid lines) S-parameters of the Alenia P11 in the 0.5 - 26 GHz band. In order to check the large-signal/small-signal consistency of the model, in this figure the "modeled" S-parameters are computed by HB analysis, with the device excited by a very small sinusoidal signal (-50 dBm) superimposed on the bias sources.


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## REFERENCES


[1] A. Winslow and R. J. Trew, "Principles of large-signal MESFET operation", *IEEE Trans. Microwave Theory Tech.*, Vol. 42, June 1994, pp. 935-942.

[2] V. Rizzoli, A. Costanzo, and G. Muzzarelli, "A universal electrothermal FET model suitable for general large-signal applications", *Proc. 26th European Microwave Conf.* (Prague), Sep. 1996, pp. 251-255.

[3] V. Rizzoli *et al.*, "Unambiguons parameter extraction for nonlinear FET models based on physical constraints", *Proc. INMMC'96*, Duisburg, Oct. 1996, pp. 149-154.

[4] V. Rizzoli *et al.*, "An electrothermal functional model of the microwave FET suitable for nonlinear simulation", *Int. Journal Microwave Millimeter-Wave Computer-Aided Eng.*, Vol. 5, March 1995, pp. 104-121.

[5] M. C. Foisy, P. E. Jeroma, and G. H. Martin, "Large-signal relaxation-time model for HEMTs and MESFETs", *1992 IEEE MTT-S Int. Microwave Symp. Digest*, Albuquerque, NM, June 1992, pp. 251-254.[5]

[6] R. R. Daniels, A. T. Yang, and J. P. Harrang, "A universal large/small signal 3-terminal FET model using a nonquasi-static charge-based approach", *IEEE Trans. Electron Devices*, Vol. 40, Oct. 1993, pp. 1723-1729.

[7] D. E. Root, "Measurement-based active device modeling for circuit simulation", *Proc. Workshop on Advanced Microwave Devices, Characterisation and Modelling*, Madrid, Sept. 1993.

[8] W. R. Curtice, "Intrinsic GaAs MESFET equivalent circuit models generated from two-dimensional simulation", *IEEE Trans. Computer-Aided Design*, Vol. 8, Apr. 1989, pp. 395-402.

[9] E. D. Ostroff *et al*., *Solid-State Radar Transmitters*. Dedham: Artech House, 1985.

[10] G. Kompa, "Modeling of dispersive microwave FET devices using a quasi-static approach", *Int. Journal Microwave Millimeter-Wave Computer-Aided Eng*., Vol. 5, May 1995, pp. 173-194.

[11] V. Rizzoli *et al*., "State-of-the-art harmonic-balance simulation of forced nonlinear microwave circuits by the piecewise technique", *IEEE Trans. Microwave Theory Tech*., Vol. 40, Jan. 1992, pp. 12-28.


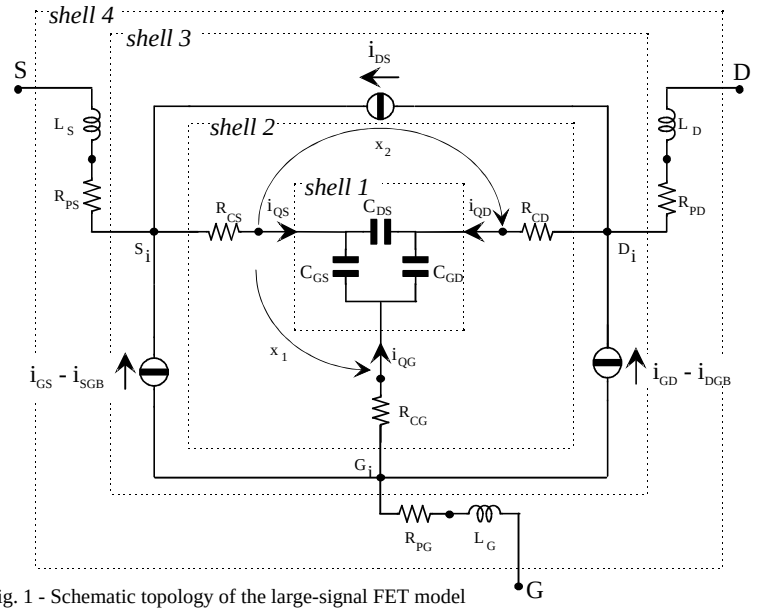


Fig. 1 - Schematic topology of the large-signal FET model

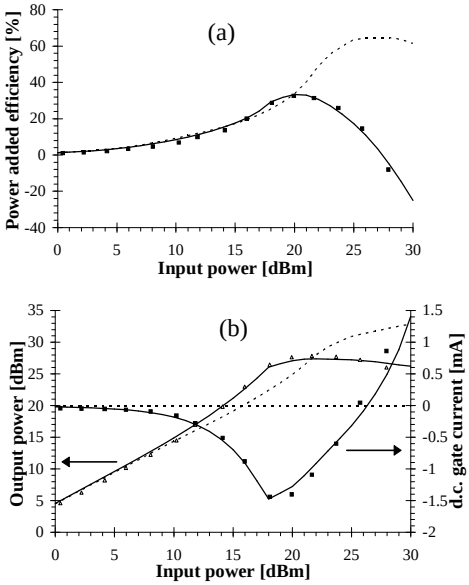


Fig. 3 - Ideal (dashed lines), predicted (solid lines) and measured (points) device performance @ $v_{DS}$ = 12 V, $v_{GS}$ = -4 V.

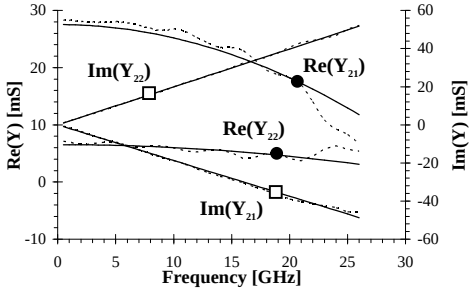


Fig. 2 - Real (●) and imaginary (□) parts of the extracted (dashed lines) and computed (solid lines) intrinsic admittance parameters @ $v_{DS}$ = 5 V,$v_{GS}$ = -3.4 V [freq. 0.5 ÷26 GHz].

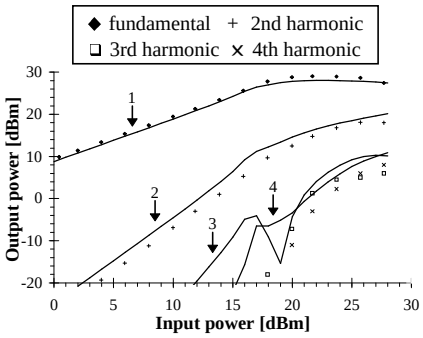


Fig. 4 - Predicted (lines) and measured (points) output harmonic levels @ $v_{DS}$ = 10 V, $v_{GS}$ = -2 V [fundamental frequency 2.5 GHz].

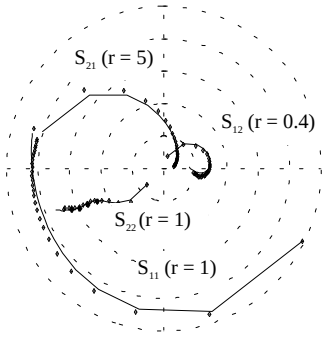


Fig. 5 - S-parameters @ $v_{DS}$ = 1 V, $v_{GS}$ = -1.2 V [freq. 0.5 ÷ 26 GHz] [◆ measured —modeled].